WE CLAIM:

1. An integrated circuit comprising:

a conductive plug having an upper surface, the conductive plug formed in a lower insulating layer and having a first width;

a conductive line having a lower portion, the conductive line formed over the conductive plug; and

an isolation layer formed between the conductive plug and the conductive line, the isolation layer comprising an opening through which the lower portion of the conductive line extends to make electrical contact with the upper surface of the conductive plug, the opening having a second width smaller than the first width of the conductive plug, wherein the isolation layer electrically isolates one or more outer regions of the upper surface of the conductive plug from other nearby conductive lines.

2. The integrated circuit of Claim 1, wherein the conductive plug comprises tungsten.

3. The integrated circuit of Claim 1, wherein the width of the conductive plug is between about 50 nm and about 300 nm.

4. The integrated circuit of Claim 1, further comprising an upper insulating layer overlying the isolation layer and between the conductive line and an adjacent conductive line.

5. The integrated circuit of Claim 1, wherein the conductive line comprises aluminum.

6. The integrated circuit of Claim 5, wherein the conductive line further comprises a titanium layer and a titanium nitride layer.

7. The integrated circuit of Claim 1, wherein the conductive line has a width between about 100 nm and about 120 nm.

8. The integrated circuit of Claim 1, wherein the conductive line is separated from an adjacent conductive line by less than about 110 nm.

9. The integrated circuit of Claim 1, wherein the isolation layer comprises TEOS.

10. The integrated circuit of Claim 1, wherein the isolation layer comprises silicon nitride.

11. The integrated circuit of Claim 1, wherein the isolation layer has a thickness between about 5 nm and about 100 nm.

12. The integrated circuit of Claim 11, wherein the isolation layer has a thickness between about 10 nm and 50 nm.

13. A system including an integrated circuit, comprising:

a metal plug;

a dielectric layer having a thickness between about 5 nm and about 100 nm, wherein the dielectric layer comprises an opening formed over the metal plug; and

a metal line having a lower portion that extends through the opening to make electrical contact with the metal plug.

14. The system of Claim 13, wherein the metal plug comprises tungsten.

15. The system of Claim 13, wherein the dielectric layer has a thickness between about 10 nm and 50 nm.

16. The system of Claim 13, wherein the dielectric layer has a thickness between about 20 nm and 30 nm.

17. The system of Claim 13, wherein the metal line comprises aluminum.

18. The system of Claim 13, wherein the dielectric layer comprises TEOS.

19. The system of Claim 13, wherein the dielectric layer comprises silicon nitride or BPSG.

20. A metallization scheme for an integrated circuit, comprising:

a plurality of metal plugs at a first level; and

a plurality of metal lines formed above the plurality of metal plugs at a second level, wherein the metal lines are vertically separated from the metal plugs by a distance between about 5 nm and 100 nm except at positions directly over the metal plugs.

21. The metallization scheme of Claim 20, wherein the metal lines include integral lower extensions at the positions over the metal plugs.

22. The metallization scheme of Claim 21, wherein the integral lower extensions have a width smaller than a width of the metal plugs.

23. A method of forming an integrated circuit interconnect, comprising:

providing an insulating layer as a blanket layer;

forming a first photoresist film over the insulating layer;

exposing the first photoresist film to radiation through a first mask reticle at a first radiation exposure level;

etching a via in the insulating layer;

forming a conductive plug within the via;

depositing an isolation layer over the insulating layer and the conductive plug;

forming a second photoresist film over the isolation layer;

exposing the second photoresist film to radiation through the first mask reticle at a second radiation exposure level;

etching an opening in the isolation layer over the conductive plug, the opening having a width narrower than that of the conductive plug; and

forming a conductive line over the opening such that the conductive line makes electrical contact with the conductive plug through the opening.

24. The method of Claim 23, wherein the insulating layer comprises BPSG.

25. The method of Claim 23, wherein the first photoresist film has a thickness within the range of about 500 nm to about 1,500 nm.

26. The method of Claim 25, wherein the second photoresist film has a thickness within the range of about 100 nm to about 500 nm

27. The method of Claim 23, wherein the first radiation exposure level falls within the range of about 10 mJ/cm^2 to about 90 mJ/cm^2.

28. The method of Claim 27, wherein etching a via in the insulating layer comprises dry etching.

29. The method of Claim 23, wherein the second radiation exposure level is lower than the first radiation exposure level.

30. The method of Claim 29, wherein the second radiation exposure level is more than about 5% below the first radiation exposure level.

31. The method of Claim 30, wherein the second radiation exposure level is about 10% to about 15% below the first radiation exposure level.

32. The method of Claim 23, wherein forming a conductive plug comprises performing a CMP process.

33. The method of Claim 23, wherein the conductive plug comprises tungsten.

34. The method of Claim 23, wherein the isolation layer comprises a form of silicon oxide.

35. The method of Claim 23, wherein the isolation layer comprises silicon nitride.

36. The method of Claim 23, wherein etching a via in the isolation layer comprises dry etching.

37. The method of Claim 23, wherein etching a via in the isolation layer comprises wet etching.

38. The method of Claim 23, wherein forming a conductive line comprises blanket metal deposition and subsequent etching.

39. The method of Claim 23, wherein the conductive line comprises aluminum.

40. A method of forming a conductive bridge between a metal line and a conductive plug, comprising:

forming an insulating layer having a thickness of less than about 100 nm;

forming an opening within the insulating layer; and

filling the opening with metal.

41. The method of Claim 40, wherein the insulating layer comprises an oxide.

42. The method of Claim 40, wherein the insulating layer comprises silicon nitride.

43. The method of Claim 40, wherein the metal comprises aluminum.

44. The method of Claim 40, wherein filling the via with metal comprises depositing a blanket metal layer.

45. The method of Claim 44, further comprising etching the blanket metal layer to form the metal line.

46. The method of Claim 40, wherein forming the opening within the insulating layer comprises employing a photolithography reticle that is also employed to define the conductive metal plug.

47. The method of Claim 46, wherein the insulating layer is deposited directly over the conductive plug.

48. A method of forming an integrated circuit element, comprising:

using a first mask to form a first via by subjecting a first photoresist film to radiation through the first mask at a first radiation exposure level;

depositing a first metal into the first via;

using the first mask a second time to form a second via by subjecting a second photoresist film to radiation through the first mask at a second radiation exposure level; and

depositing a second metal into the second via.

49. The method of Claim 48, wherein the first photoresist film has a thickness within the range of about 500 nm to about 1,500 nm.

50. The method of Claim 48, wherein the first radiation exposure level falls within the range of about 35 mJ/cm^2 to about 41 mJ/cm^2.

51. The method of Claim 48, wherein the first metal comprises tungsten.

52. The method of Claim 48, wherein the second photoresist film has a thickness within the range of about 100 nm to about 500 nm.

53. The method of Claim 48, wherein the second radiation exposure level is less than the first radiation exposure level and the first and second photoresist films are positive photoresists.

54. The method of Claim 53, wherein the second radiation exposure level is more than about 5% below the first radiation exposure level.

55. The method of Claim 54, wherein the second radiation exposure level is about 10% to about 15% below the first radiation exposure level.

56. The method of Claim 48, wherein the second radiation exposure level is more than the first radiation exposure level and the first and second photoresist films are negative photoresists.

57. The method of Claim 56, wherein the second radiation exposure level is more than about 5% above the first radiation exposure level.

58. The method of Claim 48, wherein the second metal comprises aluminum.

59. The method of Claim 58, further comprising etching the second metal above the second via to define a plurality of metal lines.

60. The method of Claim 59, further comprising depositing an insulating layer between the metal lines and above an isolation layer in which the second via was etched.

61. A method of forming a plurality of conductive lines, comprising:

forming a plurality of vias in a dielectric layer having a thickness of less than about 100 nm;

depositing a conductive material over the dielectric layer such that the vias are filled with the conductive material and a conductive layer is formed over the dielectric layer and the filled vias; and

etching the conductive layer to form a plurality of conductive lines above the dielectric layer and the filled vias.

62. The method of Claim 61, wherein the conductive material comprises aluminum.